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[Using on-the-Fly Verification Techniques for the.. - Jean-Claude Fernandez \(1996\) \(Correct\)](#)

transition systems. Formal Methods in System **Design**, 1:251-273, 1992. Kluwer Academic Publishers. partially supported by an industrial contract with **Verilog** in a study for the french DGA (Direction automatique de s'equences de test 11 from **Verilog** as an SDL [3] front-end which produces state ftp.inrialpes.fr/pub/INRIA/projets/VASY/publications/cadp/Fernandez-Jard-Jeron-et-al-96-a.ps.Z

[Bisimulation Minimization in an Automata-Theoretic.. - Kathi Fisler \(1998\) \(Correct\) \(2 citations\)](#)

the required BDDs are prohibitively large for most **designs**. We revisit bisimulation minimization, this time www.cs.rice.edu/~kfisler/Pubs/fmcad98.ps.gz

[The START-VOYAGER Parallel System - Ang \(1998\) \(Correct\) \(1 citation\)](#)

a novel protection scheme which improves upon past **designs** by not requiring strictly synchronized Performance predictions based on synthesized **Verilog** code show START-VOYAGER's novel message passing derived from simulation with synthesizable **Verilog** code (Section 5)2. Requirements Our basic csg-ftp.lcs.mit.edu/pub/papers/csgmemo/memo-416.ps.gz

[The Synchronous System Description Language PURR - Kropf, Ruf, Schneider, Wild \(1998\) \(Correct\)](#)

of Computer Science, Institute for Computer **Design** and Fault Tolerance (Prof. D. Schmid)P.O. Box description languages such as VHDL [10] or **Verilog** [16]Both languages are dedicated to the to hardware description languages like VHDL or **Verilog**, these languages have been **designed** with the goethe.ira.uka.de/~schneider/my_papers/KRSW98a.ps.gz

[SpecSyn: An Environment Supporting the.. - Gajski, Vahid.. \(1998\) \(Correct\) \(2 citations\)](#)

Paradigm for Hardware/Software System **Design** Daniel D. Gajski, Frank Vahid, Sanjiv Narayan www.cs.ucr.edu/~vahid/courses/269_f98/specsyn_tvlsi97.ps

[Reversible Computing for Energy Efficient and Trustable.. - Knight, Jr. \(1995\) \(Correct\)](#)

transactional issues, and programming language **design** which also make fully reversible computer architecture (year 1)ffl MIT will develop full **Verilog** simulations for the reversible architecture, circuits (years 1-2)ffl MIT will develop **Verilog** simulations of a dynamically reconfigurable www.ai.mit.edu/people/cvieri/proposal.ps

[PAM-Blox: High Performance FPGA Design for Adaptive Computing - Mencer, Morf, Flynn \(1998\) \(Correct\) \(13 citations\)](#)

PAM-Blox: High Performance FPGA **Design** for Adaptive Computing Oskar Mencer, Martin arith.stanford.edu/oskar/fccm98.ps

[Statechart Methodology for the Design, Validation, and.. - Kol, Ginosar, Samuel \(1996\) \(Correct\) \(1 citation\)](#)

Statechart Methodology for the **Design**, Validation, and Synthesis of Large Scale C or Ada) or a hardware description (in VHDL or **Verilog**, at either the behavioral or RTL levels)The compiles the specification into either VHDL or **Verilog**. It can compile into either behavioral or RTL ftp.technion.ac.il/pub/supported/ee/VLSI/async-statecharts.ps.gz

[Robust, High-Speed Network Design for Large-Scale Multiprocessing - DeHon \(1993\) \(Correct\) \(1 citation\)](#)

so they can easily be extended or re-**parameterized** to solve a variety of problems. When building 1445 September, 1993 Robust, High-Speed Network **Design** for Large-Scale Multiprocessing Andr e DeHon on their synthesis tools. Cadence provided us with **Verilog**-XL for simulation. Logic Modeling Corporation www.ai.mit.edu/projects/transit/papers/robust-high-speed-networks.ps.Z

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resources. It cannot, for example, verify a **parameterized design** for all values of the parameter (such as
www-cad.eecs.berkeley.edu/~kenmcmil/papers/1999-01.ps.gz

[Application-Specific Clustered VLIW Datapaths: Early.. - Lapinskii, Jacome, de .. \(2002\)](#) [\(Correct\)](#) [\(5 citations\)](#)
VLIW Datapaths: Early Exploration on a **Parameterized Design** Space Viktor S. Lapinskii, Margarida F.
very efficiently in this abstract, **parameterized design** space. Moreover, an empirical study
www.ece.utexas.edu/%7Elapinski/publications/cade.pdf

[Fitting Curves and Surfaces with Constrained Implicit Polynomials - Keren, Gotsman \(1999\)](#) [\(Correct\)](#) [\(4 citations\)](#)
paper suggests a different approach-to **design parameterized** families of polynomials whose zero-sets
www.cs.haifa.ac.il/~dkeren/mypapers/implicit-99.pdf

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gnuplot. 89 6. Software Tools for **Parameterized Design** 6.1 wirec and xs The design entry for ACME
<ftp.cse.ucsc.edu/pub/borg/ACME/aaronf.ps.Z>

[Innovative Design as Systematic Search - Dorothy Neville Daniel \(1992\)](#) [\(Correct\)](#) [\(3 citations\)](#)
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www.cs.washington.edu/homes/weld/papers/sie-aaai93.pdf

[A Beamformer ASIC using Cordic Arithmetic - Xu, Steensma \(1997\)](#) [\(Correct\)](#) [\(2 citations\)](#)
does support neither multiprocessor nor **parameterized design** and is control oriented. So, A
www.stw.nl/prorisc/cssp97/proc/psz/xu.ps.gz

[Utilizing Rapid Prototyping To Enhance Undergraduate.. - Stamper, Dekker \(2000\)](#) [\(Correct\)](#) [\(1 citation\)](#)
from the mannequin to update their **parameterized design**, and then built their halo systems using
fie.engrng.pitt.edu/fie2000/papers/1163.pdf

[Design Space Exploration for The Beamformer System - Smita Bakshi Daniel \(1993\)](#) [\(Correct\)](#) [\(1 citation\)](#)
In order to do so, we first define a **parameterized design** template for the beamformer and for a FIR
we start by defining and illustrating a **parameterized design** template using several simple examples.
recluse.ics.uci.edu/pub/cad/public_ftp/cadlab-trs/1993/TR-93-34.beamformer_exploration.ps.gz

[Instruction-Processing Optimization Techniques For VLSI.. - Bunda \(1993\)](#) [\(Correct\)](#) [\(1 citation\)](#)
these decisions. Within the framework of a **parameterized design** for a RISC instruction processor,
<ftp.cs.utexas.edu/pub/techreports/tr93-19.ps.Z>

[Exploring the Design Space of LUT-based Transparent.. - Yehia, Clark, Mahlke.. \(2005\)](#) [\(Correct\)](#)
not a single design, but rather specifies a **parameterized design** space that offers complex tradeoffs
www.eecs.umich.edu/~ntclark/papers/cases05.pdf

[Learning Spectral Graph Segmentation - Timothee Cour University](#) [\(Correct\)](#)
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from Conjoint analysis Our fully **parameterized design** matrix consists of 15 columns
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Barroso, L.A.; Iman, S.; Dubois, M.; Ramamurthy, K.;
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Volume 28, Issue 2, Feb. 1995 Page(s):26 - 34

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☐ 2. **Coverage metrics for functional validation of hardware designs**

Tasiran, S.; Keutzer, K.;

[Design & Test of Computers, IEEE](#)

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[BOOK] **VHDL for Programmable Logic**

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K Skahill - 1996 - Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA

[Cited by 101](#) - [Web Search](#) - [Library Search](#)

[BOOK] **High-level synthesis: introduction to chip and system design**

DD Gajski, ND Dutt, CHW Allen, YLL Steve - 1992 - Kluwer Academic Publishers Norwell, MA, USA

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A Reuse Scenario for the VHDL-Based Hardware Design Flow - group of 7 »

V Preis, R Henftling, M Schütz, S März-Rössel - Proceedings of EURO-DAC in Brighton, 1995 - doi.ieeecs.org

... the **parameter** set. 0 **Design** management information: eg model type, reports, revision control, automated checks. 3.1.2 VHDE Constructs for Reusability **VHDL** was ...

[Cited by 15](#) - [Web Search](#)

From VHDL to efficient and first-time-right designs: a formal approach - group of 5 »

PFA Middelhoek, SP Rajan - ACM Transactions on **Design** Automation of Electronic Systems ..., 1996 - portal.acm.org

... From **VHDL** to Efficient and First-Time-Right ... Partitioning restricts the **design** space that can be ... the application domain and the **parameterized** target architecture ...

[Cited by 11](#) - [Web Search](#)

Increasing design quality and engineering productivity through design reuse - group of 2 »

E Girczyc, S Carlson - Proceedings of the 30th international conference on **Design** ..., 1993 - portal.acm.org

... Next, **designs** can be **parameterized**. While a ... In an FILD methodology, functionality can also be **parameterized** without increasing **design** cost if ...

[Cited by 43](#) - [Web Search](#)

Parameterized IP core design

Z Junchao, C Weiliang, W Shaojun - ASIC, 2001. Proceedings. 4th International Conference on, 2001 - ieeexplore.ieee.org

... Static parameterization is addressed by **VHDL** coding style ... To dynamic parameterization, a systematic **design** idea is ... effective to deal with **parameterized** firm or ...

[Cited by 7](#) - [Web Search](#)

Exploring architectures for volume visualization on the Teramaccustom computer - group of 3 »

WB Culbertson, R Amerson, RJ Carter, P Kuekes, G ... - FPGAs for Custom Computing Machines, 1996. Proceedings. IEEE ..., 1996 - ieeexplore.ieee.org

... a process for creating Tera- mac **designs** in **VHDL**. ... Tsutsuji **designs** are hier- archies of block ... have recently found it useful for creating **parameterized designs**. ...

[Cited by 12](#) - [Web Search](#)

Embedded computer architecture and automation - group of 7 »

R Rau, B Schlansker - Computer, 2001 - ieeexplore.ieee.org

... user specifies a set of values that each **parameter** can assume. ... architects a set of Pareto- optimal system **designs** and emits the struc- tural **VHDL** for the ...

[Cited by 22](#) - [Web Search](#) - [BL Direct](#)

PEAS-III: An ASIP Design Environment - group of 5 »

M Itoh, S Higaki, J Sato, A Shiomi, Y Takeuchi, A ... - ... Conference on Computer **Design**: VLSI in Computers & ..., 2000 - doi.ieeecs.org

... be evalu- ated using the generated synthesizable **VHDL**. ... of this section describes each **design** step in ... In the architecture **parameter** setting phase, the designer ...

[Cited by 29](#) - [Web Search](#)

[PS] **A synthesizable VHDL coding of a genetic algorithm** - group of 5 »

SD Scott, S Seth, A Samal - Practical Handbook of Genetic Algorithms: Complex Coding ..., 1999 - cse.unl.edu

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[\[BOOK\] ... of Verifiable Rtl Design: A Functional Coding Style Suporting Verification Processes in Verilog - group of 4 »](#)

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L Bening, H Foster - 2001 - books.google.com

... 124 6.4.2 Model Checking and **Parameterized** Modules 126 6.4.3 ... RTLs such as **Verilog** improve the ability of the designer to communicate the **design** intent as ...

[Cited by 46 - Web Search](#)

[Increasing design quality and engineering productivity through design reuse - group of 2 »](#)

E Girczyc, S Carlson - Proceedings of the 30th international conference on **Design** ..., 1993 - portal.acm.org

... Next, **designs** can be **parameterized**. While a ... In an FILD methodology, functionality can also be **parameterized** without increasing **design** cost if ...

[Cited by 43 - Web Search](#)

[Verischemelog: Verilog embedded in Scheme - group of 3 »](#)

J Jennings, E Beuscher - Proceedings of the 2nd conference on Domain-specific ..., 2000 - portal.acm.org

... **Verilog** has a small macro language, essentially based on ... Common **design** elements in digital systems include ... state machines (which are **parameterized** by their ...

[Cited by 8 - Web Search](#) - [BL Direct](#)

[Parameterized IP core design](#)

Z Junchao, C Weiliang, W Shaojun - ASIC, 2001. Proceedings. 4th International Conference on, 2001 - ieeexplore.ieee.org

... The **parameter** typically appears as part of the SoC **design** ... They are common in the **design** of the control Page ... needs IF providers to support both **Verilog** and VFIDL ...

[Cited by 7 - Web Search](#)

[CSCI 320 Computer Architecture Handbook on Verilog HDL - group of 63 »](#)

DC Hyde - Computer Science Department of Bucknell University, Aug, 1997 - karmak.org

... scope(<name>); The <name> **parameter** must be ... Singh, Y. Trivedi, R. Madhaven and W. Stapleton, Digital **Design** and Synthesis with **Verilog** HDL, published ...

[Cited by 10 - Cached](#) - [Web Search](#)

[AHD languages-a must for time-critical designs - group of 2 »](#)

BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org

... be represented, VHDL-A and **Verilog-A** are ... guages intended to solve the **design** representation problems ... These models are typically **parameterized** where there is ...

[Cited by 6 - Web Search](#)

[Trends in CAD of analog ICs](#)

BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org

... New developments in AHDs have seen the emergence of standards for VHDL-A and **Verilog-A** to ... Model **parameter** extraction and **design** methodologies Inadequate ...

[Cited by 14 - Web Search](#) - [BL Direct](#)

[Three decades of HDLs. II. Conlan through Verilog - group of 4 »](#)

D Borrione, R Piloty, D Hill, KJ Lieberherr, P ... - **Design** & Test of Computers, IEEE, 1992 - ieeexplore.ieee.org

... in the mid-1 970s through the development of **Verilog** in the ... evaluate and write assertions either after the interface/ **parameter** list of a **design** entity or ...

[Cited by 5 - Web Search](#)

[Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - group of 9 »](#)

CE Cummings - ... , San Jose, CA, www. sunburst-design. com/papers, March, 2001 - sunburst-design.com

... This time window is specified as a **design parameter** precisely to keep a data signal from changing too close to another synchronizing signal that could cause ...

[Cited by 5 - View as HTML](#) - [Web Search](#)

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Our proposed **design** methodology to support the architectural **design** trade-off is to develop a. **parameterized Verilog** Framework. This is shown in figure 2. ...

www.engr.sjsu.edu/electrical/master_proposal_example.pdf - [Similar pages](#)

[PDF] New Verilog-2001 Techniques for Creating Parameterized Models (or ...File Format: PDF/Adobe Acrobat - [View as HTML](#)

of any parameters until all of the **Verilog** input files have. been read, because the last file read might change every. single **parameter** in the **design**! ...

www.sunburst-design.com/papers/CummingsHDLCON2002_Parameters_rev1_2.pdf -

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[PDF] Verilog-2001 Behavioral and Synthesis Enhancements Revised - April ...File Format: PDF/Adobe Acrobat - [View as HTML](#)

change any **parameter** on any module. Translation - when compiling a **Verilog design**, none of the. parameters in any module are fixed until the last **Verilog** ...

www.sunburst-design.com/papers/CummingsHDLCON2001_Verilog2001.pdf -

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Creating Verilog HDL Designs for Use with MAX+PLUS II Software

Instantiate any MAX+PLUS II-supported logic function in your **Verilog** HDL **design**. You can enter the following functions: **Parameterized** and non-**parameterized** ...

www.altera.com/support/software/eda_maxplus2/synplty/vlog/creatv.html - 27k -

[Cached](#) - [Similar pages](#)

Verilog HDL: Parameterized Counter

Altera offers users **design** examples for use in **designs** for Altera devices. ... **Verilog** HDL: **Parameterized** Counter. This example shows how to instantiate an ...

www.altera.com/support/examples/verilog/ver_check_lpm.html - 22k -

[Cached](#) - [Similar pages](#)

SOCcentral: New Verilog-2001 Techniques for Creating Parmeterized ...

With respect to coding **parameterized Verilog** models, two **Verilog** constructs that are ...

Access the entire document on the Sunburst **Design**, Inc. website. ...

www.soccentral.com/results.asp?CategoryID=205&EntryID=1112 - 20k -

[Cached](#) - [Similar pages](#)

SoftJin Technologies :: Enabling Electronic Design

Compliant with IEEE 1364 **Verilog** standard • Supports behavioral, RTL and netlist description • Supports **parameterized design** ...

www.softjin.com/html/verilog.htm - 18k - [Cached](#) - [Similar pages](#)

IP Configuration Management with Abstract Parameterizations

The main focus of CoMAP is on VHDL and **Verilog** based hardware **design** flows, but its modular **design** enables the integration of any **parameter** related language ...

www.us.design-reuse.com/articles/article5327.html - 70k - [Cached](#) - [Similar pages](#)

[PDF] Microsoft PowerPoint - L03-Verilog-Design-Examples.pptFile Format: PDF/Adobe Acrobat - [View as HTML](#)

programming will be posted this week. 6.375 Spring 2006 • L03 **Verilog** 2 - **Design** Examples • 3. **Verilog** **Design** Examples. • **Parameterized** Static Elaboration ...

csg.csail.mit.edu/6.375/handouts/lectures/L03-Verilog-Design-Examples-4up.pdf -

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[\[BOOK\] Advanced programming in the UNIX environment - group of 5 »](#)

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WR Stevens... - 1992 - yendor.com

... and raise Functions * alarm and pause Functions * **Signal Sets** * sigprocmask ... Appendix

B. Miscellaneous Source Code Our **Header File** * Standard Error Routines. ...

[Cited by 392](#) - [Cached](#) - [Web Search](#) - [Library Search](#)

[\[BOOK\] Introduction to **signal processing** - group of 4 »](#)

SJ Orfanidis - 1996 - ece.rutgers.edu

... **Signal** averaging ... generator (interpolation) DFT/FFT Functions bitrev.c - bit reversed

index complex.c - complex arithmetic in C cmplx.h - **header file** for complex ...

[Cited by 222](#) - [Cached](#) - [Web Search](#) - [Library Search](#)

[The MIT-BIH Arrhythmia Database on CD-ROM and software for use with it](#)

GB Moody, RG Mark, C MIT - Computers in Cardiology 1990. Proceedings., 1990 - ieeexplore.ieee.org

... Each **signal file** contains two signals sampled at 360 Hz. '**Header**' files include

information about the leads used, the patient's age, sex, and medi ...

[Cited by 65](#) - [Web Search](#)

[The Koala component model for consumer electronics software - group of 3 »](#)

R van Ommering, F van der Linden, J Kramer, J ... - Computer, 2000 - ieeexplore.ieee.org

... This **signal** is fed to a high-end input processor (HIP) that produces decoded ... For

each module, Koala generates a **header file** with renaming macros, as shown in ...

[Cited by 188](#) - [Web Search](#) - [BL Direct](#)

[AFNI: software for analysis and visualization of functional magnetic resonance neuroimages - group of 8 »](#)

RW Cox - Comput Biomed Res, 1996 - afni.nimh.nih.gov

... in AFNI are organized into "datasets." A dataset is a 3D brick of 16-bit values,

with some associated information stored in a separate **header file**. ...

[Cited by 753](#) - [Web Search](#) - [BL Direct](#)

[\[PS\] System Level Design Using the SystemC Modeling Platform](#)

J Gerlach, W Rosenstiel - Workshop on System Design Automation SDA, 2000 - www-ti.informatik.uni-tuebingen.de

... 5 shows the corresponding source code **file**. In the top-level routine, all process

header files and the ... object, which is a special **signal**, is instantiated. ...

[Cited by 38](#) - [View as HTML](#) - [Web Search](#)

[Development of the polysomnographic database on CD-ROM - group of 5 »](#)

Y Ichimaru, GB Moody - Psychiatry and Clinical Neurosciences, 1999 - Blackwell Synergy

... record has a **header file**, which contains general information about the record such

as its length, gains and offset of each physiological **signal**, data structure ...

[Cited by 11](#) - [Web Search](#) - [BL Direct](#)

[A database for evaluation of algorithms for measurement of QT and other waveform intervals in the ECG - group of 3 »](#)

P Laguna, RG Mark, A Goldberg, GB Moody - Computers in Cardiology 1997, 1997 - ieeexplore.ieee.org

... Each record includes a **signal file** (record.dat, where record is the record name),

a **header file** (record.heg, describing the format of the **signal file**), and sev ...

[Cited by 37](#) - [Web Search](#) - [BL Direct](#)

[A stream input-output system - group of 28 »](#)

DM Ritchie - AT&T Bell Laboratories Technical Journal, 1984 - cm.bell-labs.com

... from input and output queues after a **signal** or on ... into data blocks starting with

a **header** giving the ... communicates through the terminal module, a **file pair**, and ...

[Cited by 211](#) - [Cached](#) - [Web Search](#)

Scholar

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[PS] System Level Design Using the SystemC Modeling Platform

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J Gerlach, W Rosenstiel - Workshop on System Design Automation SDA, 2000 - www-ti.informatik.uni-tuebingen.de

... This is different to languages like **Verilog** that only ... 5 shows the corresponding source code **file**. In the top-level routine, all process **header** files and the ...

[Cited by 38](#) - [View as HTML](#) - [Web Search](#)

Hardware Object Programming on the EVC1-a Reconfigurable Computer - group of 4 »

S Casselman, M Thornburg, J Schewel - FPGAs for Rapid Board Development and Reconfigurable ..., 1995 - arco.unex.es

... via schematic and VHSIC Hardware Description Language (VHDL) or **Verilog** hardware description ... The rawbits **file** is converted into a .h **header file** by a program ...

[Cited by 4](#) - [View as HTML](#) - [Web Search](#)

[BOOK] The Complete Verilog Book

V Sagdeo - 1998 - books.google.com

... one to define text substitutions and to include **files**, which are defined in ... Synthesis is an essential part of today's design process, and **Verilog** HDL usage for ...

[Cited by 7](#) - [Web Search](#) - [Library Search](#)

[BOOK] Principles of Verilog Pli

S Mittra - 1999 - books.google.com

... A PLI ROUTINE 23.1 Step I: Including the **header files** 33.2 Step ... err_intercept 53.3.4 veriusertfs 3.3.5 pli.tab **file** in VCS environment ... FUNDAMENTALS OF VERILOG FL ...

[Cited by 8](#) - [Web Search](#) - [Library Search](#)

The use of SystemC for design verification and integration test of IP-cores - group of 6 »

A Fin, F Fummi, D Signoretto - ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE ..., 2001 - ieeexplore.ieee.org

... view the core interface (the class declaration in the **header file**) and the ... descriptions to very accurate gate-level representations (VHDL or **Verilog**) by using ...

[Cited by 4](#) - [Web Search](#)

Exploiting the Power of Vera: Creating Useful Class Libraries

J Bergeron, D Simmons - Proceedings of Synopsys Users Group, 2000 - vlsidsp.el.yuntech.edu.tw

... In **Verilog**, global variables are the norm, so **Verilog** programmers may have to learn to resist the ... First, one of the **header file** must be generated manually. ...

[Cited by 2](#) - [View as HTML](#) - [Web Search](#)

SystemC Overview - group of 2 »

M Ganguly - Synopsys Inc, 2001 - www-cad.eecs.berkeley.edu

... **Verilog** VHDL Co-sim Interface **Verilog** VHDL Co-sim Interface Import Export Page 30. Testbench // **Header File** #include "systemc.h" SC_MODULE(adder_reg_tb) { ...

[Cited by 1](#) - [View as HTML](#) - [Web Search](#)

"full_case parallel_case", the Evil Twins of Verilog Synthesis - group of 4 »

CE Cummings - 1999 - sunburst-design.com

... Inferred memory devices in process in routine mux3a line 7 in **file** '.../mux3a.v ... recognize two directives when added to the end of a **Verilog case header**. ...

[Cited by 1](#) - [View as HTML](#) - [Web Search](#)

A Verilog to C compiler - group of 3 »

DJ Greaves - Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th ..., 2000 - ieeexplore.ieee.org

... The **Verilog** shown in ... include the housekeeping lines generated by the real compiler, which include the inclusion of "ttvinc", other **header files** and so ...

[Cited by 2](#) - [Web Search](#)

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Tip: Click to get a definition of: **signals data**

Or just click on the underlined words in the above colored bar

Blind Source Separation by Sparse Decomposition in a Signal Dictionary - group All articles Recent articles of 15 »

M Zibulevsky, BA Pearlmutter - Neural Computation, 2001 - neco.mitpress.org

... We tested two methods with these **data**. ... Let us consider finding the sparsest **signal** that can be obtained by a linear combination of the sensor **signals** $s=w^T X$...

Cited by 160 - [Web Search](#) - [BL Direct](#)

A self-describing data transfer methodology for ITS applications - group of 8 »

DJ Dailey, DF Meyers - Intelligent Transportation System, 1997. ITSC 97. IEEE ..., 1997 - ieeexplore.ieee.org

... mechanism for distributing ITS **data** to Information ... devices such as traffic **signal** controllers, envi ... sensor stations, dynamic message **signals**, highway advisory ...

Cited by 13 - [Web Search](#) - [Library Search](#) - [BL Direct](#)

A software design method for real-time systems - group of 8 »

H Gomaa - Communications of the ACM, 1984 - portal.acm.org

... to wait for an acknowledgment before Output Axis **Data** can output ... queue, as well as Stop and Resume event **signals** from the ... If so, it waits for a Resume **signal**. ...

Cited by 67 - [Web Search](#)

[book] Data compression: methods and theory

JA Storer - 1987 - Computer Science Press, Inc. New York, NY, USA

... Dictionaries, Journal of VLSI **Signal** Processing Systems ... Practical prefetching via **data** compression, ACM ... Muthukrishnan, Optimal parallel **dictionary** matching and ...

Cited by 245 - [Web Search](#) - [Library Search](#)

Building a dictionary for genomes: Identification of presumptive regulatory sites by statistical ... - group of 35 »

HJ Bussemaker, H Li, ED Siggia - Proceedings of the National Academy of Sciences, 2000 - pnas.org

... the fluctuations and thus meaningful **signals** in the ... among all segmentations of the **data**; then the ... **dictionary** does not distinguish between **signal** and background ...

Cited by 123 - [Web Search](#) - [BL Direct](#)

The PROSITE dictionary of sites and patterns in proteins, its current status - group of 7 »

A Bairoch - Nucleic Acids Res, 1993 - pubmedcentral.nih.gov

... The PROSITE **dictionary** of sites and patterns in proteins, its ... The SWISS-PROT protein sequence **data** bank ... Staden R. Computer methods to locate **signals** in nucleic ...

Cited by 709 - [Web Search](#) - [BL Direct](#)

Learning pronunciation dictionary from speech data - group of 3 »

CM Westendorf, J Jelitto - Spoken Language, 1996. ICSLP 96. Proceedings., Fourth ..., 1996 - ieeexplore.ieee.org

... the **data** base are the (unlabeled) **signals** and their ... which actually occurred in the **data** or which ... a lattice of phonemic hypotheses from the speech **signal**. ...

Cited by 8 - [Web Search](#)

... Evaluation of a Data Mining Approach to Aid Finding New Adverse Drug Reaction Signals in the WHO ... - group of 4 »

M Lindquist, M Ståhl, A Bate, IR Edwards, RHB ... - Drug Safety, 2000 - ingentaconnect.com

... programme is to identify early **signals** of safety ... It complements the previous **signal** generation procedure which in ... new system is based on a **data** mining technique ...

Cited by 32 - [Web Search](#) - [BL Direct](#)

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Computer-aided **design** of analog and mixed-**signal** integrated circuits - group of 2 [All articles](#) [Recent articles](#)

»

GGE Gielen, RA Rutenbar - Proceedings of the IEEE, 2000 - [ieeexplore.ieee.org](#)

... What is needed to expedite the analog and mixed-**signal design** process is a structured methodology and supporting CAD tools to manage the entire **design** process ...

Cited by 121 - [Web Search](#) - [BL Direct](#)

Fault **dictionary** based upon stimulus **design**

H Schreiber - Circuits and Systems, IEEE Transactions on, 1979 - [ieeexplore.ieee.org](#)

... in **signal** space, and the fault **dictionary** is constructed ... allow the dimension of the **signal** space to ... The theory of stimulus **design** for fault isolation in linear ...

Cited by 18 - [Web Search](#)

Blind Source Separation via Multinode Sparse Representation

M Zibulevsky, YY Zeevi... - Neural Computation, 2001 - [citeseer.ist.psu.edu](#)

... related documents): More All 0.3: Excitation Codebook **Design** For - Coding ... separation by sparse decomposition in a **signal dictionary** - Zibulevsky, Pearlmutter ...

Cited by 30 - [Cached](#) - [Web Search](#) - [BL Direct](#)

A theory for multiresolution **signal** decomposition: the wavelet representation - group of 16 »

SG Mallat - Pattern Analysis and Machine Intelligence, IEEE Transactions ..., 1989 - [ieeexplore.ieee.org](#)

A theory for multiresolution **signal** decomposition: the wavelet representation.

Mallat, SG Dept. of Comput. Sci., New York Univ., NY; ...

Cited by 5041 - [Web Search](#) - [Library Search](#)

Design of a linguistic statistical decoder for the recognition of continuous speech

F Jelinek, L Bahl, R Mercer - Information Theory, IEEE Transactions on, 1975 - [ieeexplore.ieee.org](#)

... **Design** of a Linguistic Statistical Decoder for ... Although the probabilities for the phonemic **dictionary** and phonological ... deter- mine for an acoustic **signal** A and ...

Cited by 60 - [Web Search](#)

A **design-for-test** methodology for active analog filters

M Soma - Test Conference, 1990. Proceedings., International, 1990 - [ieeexplore.ieee.org](#)

... Lin and Elcherif [2] studies the analog fault **dictionary** approach with ... for analog macrocircuits frequently used in VLSI and **signal** processor **designs**. ...

Cited by 85 - [Web Search](#)

Challenges in analog and mixed-**signal** fault models - group of 2 »

M Soma - Circuits and Devices Magazine, IEEE, 1996 - [ieeexplore.ieee.org](#)

... customary with past developments, however, **design** outpaces testing ... critical area of mixed-**signal** testing-and ... Analog circuits fault **dictionary**— new approaches ...

Cited by 20 - [Web Search](#) - [BL Direct](#)

Optimized **signal** expansions for sparse representation - group of 3 »

SO Aase, JH Husoy, J Skretting, K Engan - ... Acoustics, Speech, and **Signal** Processing, IEEE Transactions ..., 2001 - [ieeexplore.ieee.org](#)

... motivates our own algorithm for transform vector **design** is reported ... part, we find approximations to the training **signal** using an ini- tial **dictionary** or the ...

Cited by 11 - [Web Search](#) - [BL Direct](#)

[book] Adaptive system identification and **signal** processing algorithms

N Kalouptsidis, S Theodoridis - 1993 - Prentice-Hall, Inc. Upper Saddle River, NJ, USA

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Web-based acquisition, storage, and retrieval of biomedical signals - group of 4 »

NH Lovell, F Magrabi, BG Celler, K Huynh, H ... - Engineering in Medicine and Biology Magazine, IEEE, 2001 - [ieeexplore.ieee.org](#)

... The relational database facilitates fast schema **design** and easy maintenance. ... lection of a patient table from a set of tables in a biomedical **signals database**. ...

[Cited by 22](#) - [Web Search](#) - [BL Direct](#)

Relational database: a radiation therapy machine control software development tool

J Jacky, R Risler, S Brossard, I Kalet - Engineering in Medicine and Biology Society, 1989. Images of ..., 1989 - [ieeexplore.ieee.org](#)

... The **Signals Database** The CNTS control system includes over 1000 digital and ... documents and computer text files, including service manuals, **design** drawings and ...

[Cited by 1](#) - [Web Search](#)

Database on mRNA-Located Eukaryotic Expression Signals Influencing Translation Efficiency and ... - group of 2 »

AV Kochetov, D Grogovich, NA Kolchanov, A Sarai - GENOME INFORMATICS SERIES, 2001 - [hc.ims.u-tokyo.ac.jp](#)

... Keywords: translational **signals, database**, mRNA, enhancer 1 Introduction ... COMMENT

design of reporter GUS gene mRNA 5'UTR in experiment: first 23 nt were.. ...

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An integrated architecture for signal validation in power plants - group of 2 »

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